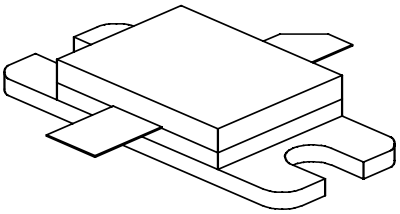
# 1214-110V

110 Watts - 50 Volts, 330µs, 10%
Radar 1200 - 1400 MHz

## GENERAL DESCRIPTION

The 1214-110V is an internally matched, COMMON BASE transistor capable of providing 110 Watts of pulsed RF output power at 330 µs pulse width, 10% duty factor across the band 1200 to 1400 MHz. This hermetically solder-sealed transistor is specifically designed for L-Band radar applications. It utilizes gold metallization and diffused emitter ballasting to provide high reliability and supreme ruggedness.

## CASE OUTLINE
## 55KT, STYLE 1



## ABSOLUTE MAXIMUM RATINGS

Maximum Power Dissipation @ 25°C 270 Watts

**Maximum Voltage and Current**

| | | |
|---|---|---|
| BVces | Collector to Emitter Voltage | 75 Volts |
| BVebo | Emitter to Base Voltage | 3.0 Volts |
| Ic | Collector Current | 8 Amps |

**Maximum Temperatures**

| | |
|---|---|
| Storage Temperature | - 65 to + 200°C |
| Operating Junction Temperature | + 200°C |

## ELECTRICAL CHARACTERISTICS @ 25 °C

| SYMBOL | CHARACTERISTICS | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Pout** | Power Out | Freq = 1200 – 1400 MHz | 110 | | 160 | Watts |
| **Pg** | Power Gain | Vcc = 50 Volts | 7.4 | | | dB |
| **ηc** | Collector Efficiency | Pin = 20 Watts | 50 | 55 | | % |
| **RI** | Input Return loss | Pulse Width = 330µs | 10 | | | dB |
| **Droop** | Droop | Duty Factor = 10% | | | 0.5 | dB |
| **Flatness** | Flatness | | | | 1.0 | dB |
| **VSWR-S** | Load Mismatch Stability | | | | 1.5:1 | |
| **VSWR-T** | Load Mismatch Tolerance | | | | 3.0:1 | |

**FUNCTIONAL CHARACTERISTICS @ 25°C**

| | | | | | | |
|---|---|---|---|---|---|---|
| **Bvces** | Collector to Emitter Breakdown | Ic = 100 mA | 75 | | | Volts |
| **Ices** | Collector to Emitter Leakage | Vce = 50 Volts | | | 10 | mA |
| **θjc**[1] | Thermal Resistance | Rated Pulse Condition | | | 0.5 | °C/W |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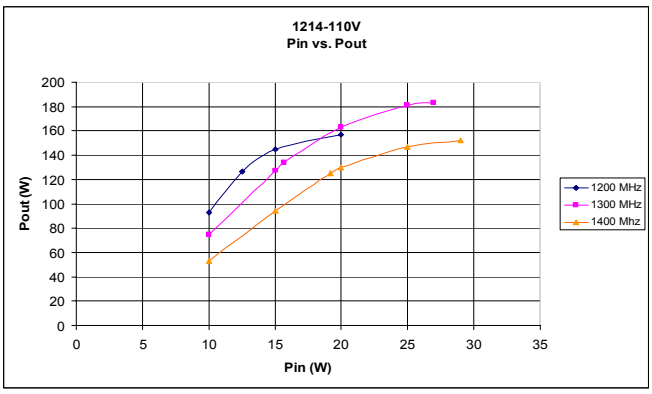
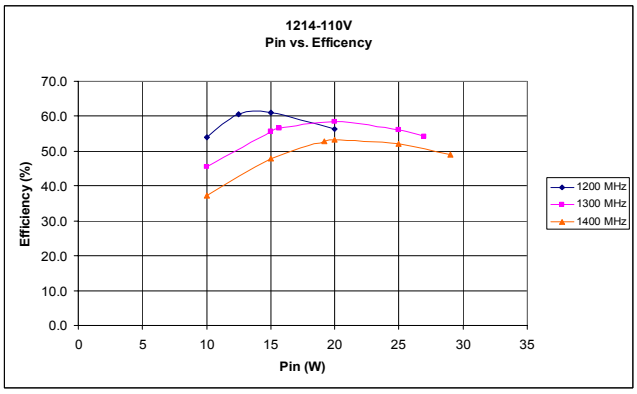
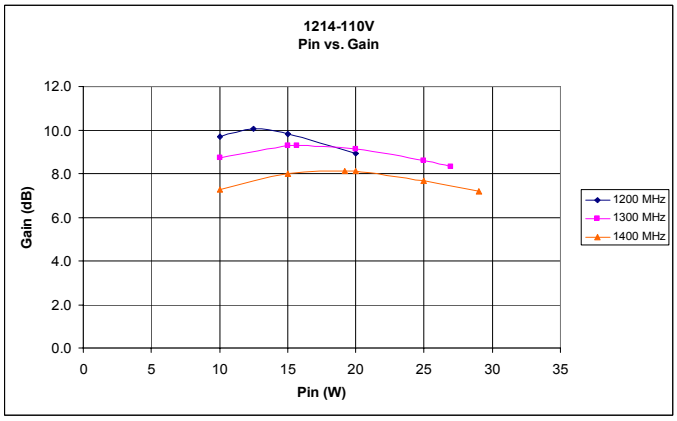
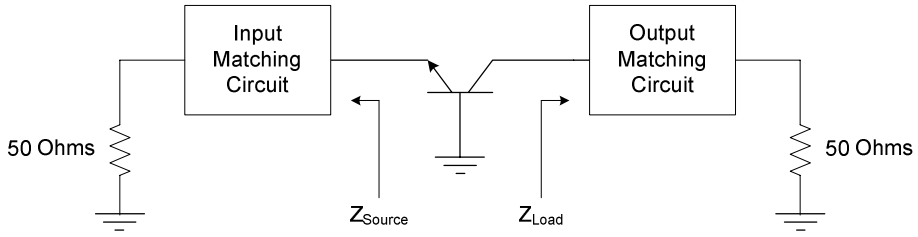
## Performance Curves




## Impedance Information




| Frequencies (MHz) | $Z_{Source}(\Omega)$ | $Z_{Load}(\Omega)$ [2] |
|---|---|---|
| 1200 | 3.36-j3.12 | 4.97+j0.15 |
| 1300 | 3.5-j2.4 | 5.33-j2.86 |
| 1400 | 3.81-j1.3 | 2.88-j3.86 |

Note 2: $Z_{Load}$ exclusive of bias circuit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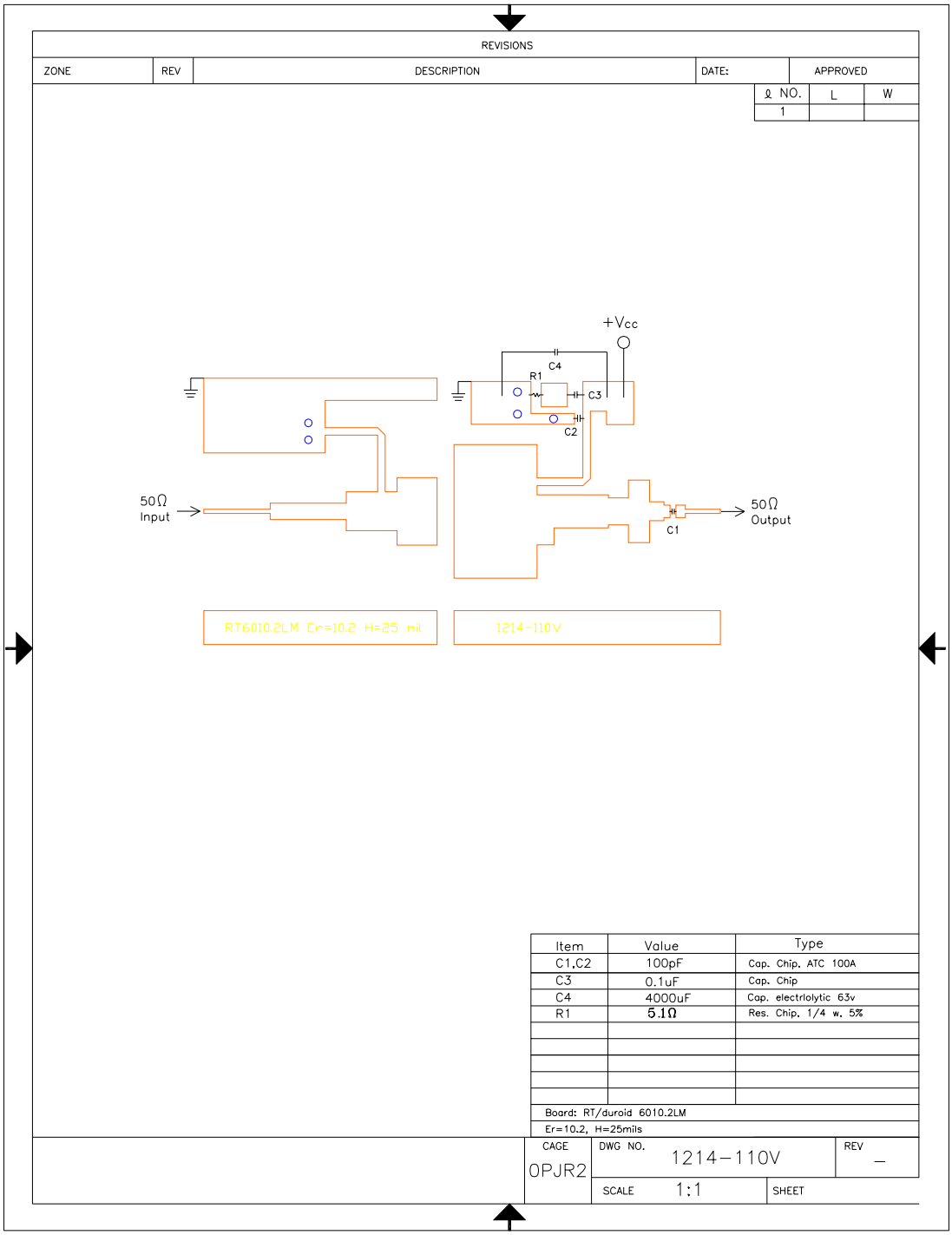
## Test Circuit



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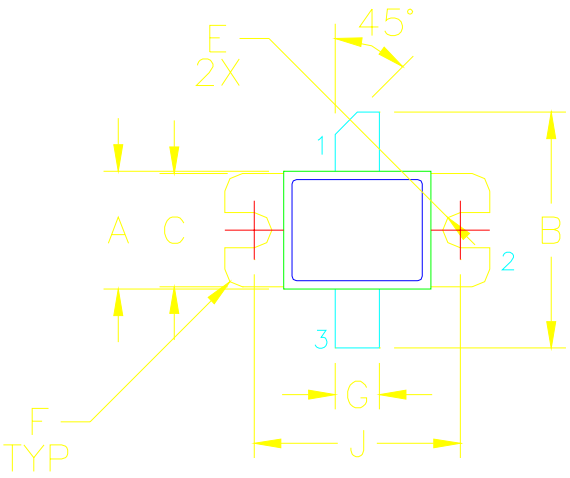
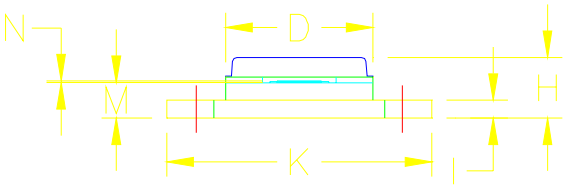
| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPROVED |

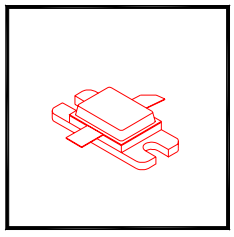



| DIM | MILLIMETER | ± TOL | INCHES | ±TOL |
|---|---|---|---|---|
| A | 10.16 | .13 | .400 | .005 |
| B | 20.32 | .76 | .800 | .030 |
| C | 9.78 | .13 | .385 | .005 |
| D | 12.70 | .13 | .500 | .005 |
| E | 1.52R | .13 | .060R | .005 |
| F | 1.52R | .13 | .060R | .005 |
| G | 3.81 | .13 | .150 | .005 |
| H | 5.84 | MAX | .230 | MAX |
| I | 1.52 | .13 | .060 | .005 |
| J | 17.78 | .13 | .700 | .005 |
| K | 22.86 | .13 | .900 | .005 |
| M | 3.05 | .13 | .120 | .010 |
| N | 0.08 | + .05 − .03 | .003 | + .002 − .001 |

STYLE 1:
PIN1 = COLLECTOR
2 = BASE
3 = EMITTER

STYLE 2:
PIN1 = COLLECTOR
2 = EMITTER
3 = BASE



| CAGE | DWG NO. | REV |
|---|---|---|
| 0PJR2 | 55KT | E |
| | SCALE 2/1 | SHEET |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